Atty Docket No.678-1315

AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS:	Dae-Gunn Jei	**GROUP ART UNIT:**	2612
SERIAL NO.:	10/777,807	**EXAMINER:**	Brown, Vernal
FILED:	February 12, 2004	**DOCKET:**	678-1315 (P11491)

FOR: **MOBILE TERMINAL CIRCUIT INCLUDING AN RFID TAG AND WIRELESS IDENTIFICATION METHOD USING THE SAME**

Mail Stop: Non-Compliant Appeal Brief
P.O. Box 1450
Alexandria, VA 22131

RESPONSE TO A NOTICE OF NON-COMPLIANT APPEAL BRIEF

Dear Sir:

In response to the Notice of Non-Compliant Appeal Brief (37 C.F.R. § 41.37) dated May 5, 2007 concerning the above-identified application, please consider the following.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postpaid in an envelope addressed to: Mail Stop, Amendment, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: June 20, 2007

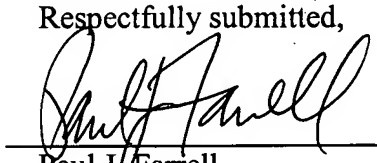
Emmanuel Ooffy

REMARKS

It is respectfully submitted that in response to the Notice of Non-Compliant Appeal Brief, the pages containing headings IX and X (Evidence Appendix and Related Proceedings Appendix) and the remainder of the claims are herewith submitted.

Should a telephone or personal interview facilitate resolution of any remaining matters, it is respectfully requested that Applicant's attorney be contacted at the number indicated below.

Respectfully submitted,



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPLICANTS:	Dae-Gunn Jei	**GROUP ART UNIT:**	2612
SERIAL No.:	10/777,807	**EXAMINER:**	Brown, Vernal
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Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF (37 C.F.R. 41.37)

Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on February 5, 2007.

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8 (a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postpaid in an envelope, addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date immediately below.

Dated: June 20, 2007

Emmanuel Coffy

REAL PARTY IN INTEREST

The real party in interest is Samsung Electronics Co. Ltd., the assignee of the subject application, having an office at 416, Maetan-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do, Republic of Korea.

RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge and belief, there are no currently pending related appeals, interferences or judicial proceedings.

STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-19.

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims cancelled: 11-13.
2. Claims withdrawn from consideration but not cancelled: none
3. Claims pending: 1-10 and 14-19.
4. Claims allowed: none
5. Claims rejected: 1-10 and 14-19.
6. Claims objected to: none.

C. CLAIMS ON APPEAL

The claims on appeal are: 1-10 and 14-19.

STATUS OF AMENDMENTS

On April 7, 2006, the Examiner issued the First Office Action on the merits (FOAM). Subsequently, an amendment was filed on July 7, 2006, in which Claims 11-13 were cancelled. The Examiner issued a second Office Action on October 4, 2006. In response to that Office Action, on January 4, 2007 a response was filed. Arguments distinguishing the invention from the references of record were presented. Original Claims 1-10 and 14-19 have not been amended.

SUMMARY OF CLAIMED SUBJECT MATTER

A. CLAIM 1 – INDEPENDENT

Claim 1 is directed to a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader. The mobile terminal circuit comprises: an antenna for communication with the RFID reader; a memory portion for storing RFID data together with mobile terminal protocol data; a codec for encoding the RFID data into RFID codec data; a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data; a processor connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec; a detector connected to the antenna and the processor, for informing the processor of approach of the RFID reader; a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion; and a second clock generator connected to the first clock generator, the codec and the modulator, for providing operation timing to the codec and the modulator.

The above circuit is described in the Specification at page 5, line 1- line 15 and page 12, lines 15-26 with reference to FIG. 4.

B. CLAIM 6 – INDEPENDENT

Claim 6 is directed to a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader. The mobile terminal circuit comprises: an antenna for communication with the RFID reader; a first clock generator for providing operation timing to each electric element of the mobile terminal circuit; an RFID module including an RFID memory for storing RFID data; a codec for encoding the RFID data into RFID codec data; a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data; and a second clock generator connected to the first clock generator, the codec and the modulator, for providing operation timing to the codec and the modulator; a power block for providing operation power to respective electric elements of the mobile terminal circuit; a processor connected to the power block, the first clock generator and the RFID module, for enabling an operation of the power block; and a detector connected to the antenna and the

processor, for informing the processor of approach of the RFID reader. The processor commands the power block to provide electric power to the RFID module, and the RFID module generates RFID modulation data using the RFID memory, the codec and the modulator.

The above mobile terminal circuit is described in the Specification at page 5, line 16-page 6, line 4.

C. CLAIM 7 – INDEPENDENT

Claim 7 is directed to a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader. The mobile terminal circuit comprises an antenna for communication with the RFID reader; a memory portion for storing RFID data together with mobile terminal protocol data; an RFID module performing an RFID function and including a second clock generator for providing RFID operation timing using a system clock output from a first clock generator; a processor connected to the memory portion and the RFID module, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the RFID module; a detector connected to the antenna and the processor, for informing the processor of approach of the RFID reader; and the first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion.

The above mobile terminal circuit is described in the Specification at page 6, line 5-line 18.

D. CLAIM 14 – INDEPENDENT

Claim 14 is directed to a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader. The mobile terminal circuit comprises: an antenna for communicating with the RFID reader; a memory portion for storing the RFID data together with mobile terminal protocol data; an RFID module for performing an RFID function and including a second clock generator for providing RFID operation timing using a system clock output from a first clock generator; a processor connected to the memory portion and the RFID module, for extracting the RFID data stored in the memory portion and delivering the extracted RFID data to the RFID module; and a detector connected to the antenna and the processor, for

informing the processor of an approach of the RFID reader.

The above mobile terminal circuit is described in the Specification at page 6, line 5-line 18 and page 12-page 14, line 10 with reference to FIGs. 1, 5 and 6.

E. CLAIM 16 – INDEPENDENT

Claim 16 is directed to a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader. The mobile terminal circuit comprising an antenna for communicating with the RFID reader; a first clock generator for providing a first operation timing to each electric element of the mobile terminal circuit; an RFID module for performing an RFID function; a power block for providing operation power to the electric elements of the mobile terminal circuit; a processor connected to the power block, the first clock generator, and the RFID module, for enabling an operation of the power block; and a detector connected to the antenna and the processor, for informing the processor of an approach of the RFID reader.

The above mobile terminal circuit is described in the Specification at page 6, line 5-line 18 and page 12-page 14, line 10 with reference to FIGs. 1, 5 and 6.

F. CLAIM 18 – INDEPENDENT

Claim 18 is directed to a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader. The mobile terminal circuit comprising an antenna for communicating with the RFID reader; a first clock generator for providing a first operation timing to each electric element of the mobile terminal circuit; a memory portion for storing the RFID data together with mobile terminal protocol data; an RFID module for processing the RFID data; a power block for providing electric power to the electric elements of the mobile terminal circuit; a processor connected to the power block, the first clock generator, the memory portion, and the RFID module, for enabling an operation of the power block, extracting the RFID data, and delivering the extracted RFID data to the RFID module; and a detector connected to the antenna and the processor, for informing the processor of an approach of the RFID reader.

The above mobile terminal circuit is described in the Specification at page 6, line 5-line 18 and page 12-page 14, line 10 with reference to FIGs. 1, 5 and 6.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. GROUND OF REJECTION 1 (Claims 1-2, 5, 14-15)

Claims 1-2, 5, 14-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kuttruff et al. (U.S. Pub. No. 2002/0080864) in view of Ohkawa (U.S. Patent No. 6,972,662).

B. GROUND OF REJECTION 2 (Claims 3-4)

Claims 3-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable Kuttruff et al. (U.S. Pub. No. 2002/0080864) in view of Ohkawa (U.S. Patent No. 6,972,662) and further in view of Pratt et al. (U.S. Pub. No. 2004/0198233).

C. GROUND OF REJECTION 3 (Claims 6-7 and 16-19)

Claims 6-7 and 16-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable Kuttruff et al. (U.S. Pub. No. 2002/0080864) in view of Ohkawa (U.S. Patent No. 6,972,662) and further in view of Twitchell Jr. (U.S. Pub. No. 2005/0215280).

D. GROUND OF REJECTION 4 (Claim 8)

Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable Kuttruff et al. (U.S. Pub. No. 2002/0080864) in view of Ohkawa (U.S. Patent No. 6,972,662) further in view of in view of Twitchell Jr. (U.S. Pub. No. 2005/0215280) and further in view of Jenkins, IV et al. (U.S. Patent No. 6,172,518).

E. GROUND OF REJECTION 5 (Claim 9)

Claim 9 stands rejected under 35 U.S.C. §103(a) as being unpatentable Kuttruff et al. (U.S. Pub. No. 2002/0080864) in view of Ohkawa (U.S. Patent No. 6,972,662) further in view of in view of Twitchell Jr. (U.S. Pub. No. 2005/0215280) and further in view of

Admitted Prior Art (APA).

F. GROUND OF REJECTION 6 (Claim 10)

Claim 10 stands rejected under 35 U.S.C. §103(a) as being unpatentable Kuttruff et al. (U.S. Pub. No. 2002/0080864) in view of Ohkawa (U.S. Patent No. 6,972,662) further in view of in view of Twitchell Jr. (U.S. Pub. No. 2005/0215280) and further in view of Pratt et al. (U.S. Pub. No. 2004/0198233).

ARGUMENT

A. GROUND OF REJECTION 1 (Claims 1-2, 5, 14-15)

A.1. Claim 1

Appellant initially shows error in the rejection of Claim 1 in that the Examiner misconstrues the teachings of the cited reference Kuttruff. Claim 1 recites, "a memory portion for storing RFID data together with mobile terminal protocol data." One of the reasons for storing RFID data together with mobile terminal protocol data is as follows. The EEPROM of the mobile terminal is an element of the memory portion. Commonly, the EEPROM stores initial setup values of the RF block, the display and voice volume, a user defined value such as address book data, and WAP (Wireless Application Protocol) data. However, as the latest Flash ROM increases in capacity, data stored in the low-speed EEPROM tends to be stored in the high-speed Flash ROM. Therefore, when a circuit's architecture makes use of both types of memory, it is common that the EEPROM has enough space capable of storing surplus data. Therefore, the present invention efficiently stores RFID data in this idle space. In rejecting this aspect of Claim 1, the Examiner cites Kuttruff teachings at paragraph 0056, as disclosing the above limitation. Appellant urges to the contrary, that these Kuttruff passages merely disclose the criteria for a changeover of the transmission method which are deposited in the processing unit, which can be preferably programmed and which has a ROM or an EEPROM, but fail to disclose a memory portion for storing RFID data together with mobile terminal protocol data, as recited in the claims of the present application.

Appellant further shows that Claim 1 of the present invention also includes a first clock generator for generating a system clock of the mobile terminal and a second clock generator for generating a clock necessary for RFID operation, using the system clock, which none of Kuttruff et al., Ohkawa et al. or Twitchell Jr. disclose.

Still further, the Examiner states Kuttruff teaches, "a storing protocol data, which represent criteria for changing over transmission and the RFID data for controlling the modulators, encoders, and decoders are stored in the EEPROM (paragraph 056)" (e.g., see, Office Action, Page 2). Nowhere in paragraph 056 or elsewhere does Kuttruff et al. disclose storing RFID data <u>together with</u> mobile terminal protocol data. Paragraph 056 of Kuttruff et al.

teaches storing on an EEPROM criteria that is needed "for a changeover of transmission method," in which the transmission method will vary depending upon closeness of an associated write/read device.

The "criteria for a changeover of transmission method" disclosed in paragraph 056 of Kuttruff et al. refers to data required to select between "signals of different standards [which] normally differ with respect to the modulation and/or the encoding." (paragraph 055 of Kuttruff et al.) At paragraph 052, Kuttruff et al. explains that its transmission standard will change "depending upon how close the chip card is to the write/read device." Accordingly, the increased amount of encoding and other data associated with the various transmission standards must be stored on the EEPROM of Kuttruff et al., which teaches away from a memory portion that stores RFID data together with mobile terminal protocol data, as in Claim 1.

Accordingly, Kuttruff cannot teach or suggest storing RFID data together with mobile terminal protocol data, as recited in Claim 1. Ohkawa fails to cure the above noted deficiencies.

Appellant has thus shown that there are missing claimed features not taught or suggested by the cited reference, and thus Claim 1 has been erroneously rejected under 35 U.S.C. §103(a). The Examiner has not established a prima facie showing of obviousness[1].

A.2. Claim 2

Appellant shows error in the rejection of Claim 2 for the reasons given above with respect to Claim 1 upon which Claim 2 depends.

A.3. Claim 5

Appellant shows error in the rejection of Claim 5 for the reasons given above with respect to Claim 1 upon which Claim 5 depends.

A.4. Claim 14

1 In rejecting claims under 35 U.S.C. §103, the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443,1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). The burden of coming forward with evidence or argument shifts to the Applicant only if the Examiner's burden is met. Id. To establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. MPEP 2143.03. See also. In re Royka, 490 F.2d 580 (C.C.P.A. 1974). If the Examiner fails to establish a prima facie case, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Appellant initially shows error in the rejection of Claim 14 for the reasons given above with respect to Claim 1. Claim 14 includes similar recitations as those contained in Claim 1.

Further, in rejecting Claim 14, the Examiner cites Figure 3 for the proposition that Ohkawa teaches the use of a separate first and second clock for the receive and transmission part of the RFID device. Appellant urges to the contrary. The Examiner acknowledges that Ohkawa is silent on teaching the second clock is connected to the encoder. (See page 4 of Office Action). In the prior art, as in Ohkawa, if the RFID reader approaches the RFID tag, the clock generator extracts a clock and provides the clock to the other elements, and the rectifier provides electric power to the elements. At this point, elements other than the rectifier are reset, so it is possible to detect the transmission time of the stored data. However, in certain environments, an unstable clock may be extracted from the carrier of the RFID reader, causing misoperation of the RFID tag. Also, detecting the data transmission point through the provided power can be affected because of the surrounding environment.

However, the present invention effectively resolves such problems. That is, since most elements of the RFID tag are arranged in the Main Processing Unit (MPU 550A), stable electric power from the power block is provided to each element of the RFID tag. In addition, the RFID tag is provided with the stable internal clock of the mobile terminal, instead of a clock extracted from the carrier of the RFID reader as in Ohkawa. The present invention is architectured such that a first clock generator is connected not only to the MPU core and the memory portion, but also to electric elements of the mobile terminal circuit, and provides operation timing to them. A system clock SCLK output from the first clock generator is provided to a second clock generator, and the second clock generator is connected to the RFID codec and the RFID modulator, and provides operation timing to them.

As can be seen, the clocking scheme of the present invention differs significantly from that of Ohkawa. The Examiner alleges that the second clock of Ohkawa is analogous to the second clock of the present invention. However, Ohkawa discloses one clock as opposed to a separate second clock generator as recited in Claim 14. The passage describing the clock arrangement of Ohkawa is reproduced below.

> Then, the phase-modulated AC wave is demodulated by the demodulator – clock generator circuit 61, and demodulated information is supplied to the processor 8.

> A carrier signal used for information transmission from the IC card 1 to the external apparatus is generated by a carrier signal generator circuit 62 which divides a frequency of the clock signal to a predetermined frequency. The carrier signal is phase-modulated with data signal from the processor 8 by a modulator 64. (emphasis added) (col. 4, lines 2-10).

As can be seen, this passage makes no mention whatsoever of any of the specific features recited in Claim 14 such as "a second clock generator for providing RFID operation timing using a system clock output from a first clock generator" nor do the teachings of the cited passage cure Kuttruff's deficiency.

It is thus further shown that Claim 14 has been erroneously rejected under 35 U.S.C. § 103, as there are additional claimed features not taught or suggested by any of the cited references.

Still further, although Claim 14 includes similar recitations as those contained in Claim 1 nevertheless the two claims are different. For example, Claim 1 recites "a codec for encoding the RFID data into RFID codec data" whereas Claim 14 does not. However, in the Office Action the Examiner lumped[2] Claims 1 and 14 together and only addressed the limitations of Claim 1; therefore the limitations of Claim 14 that are different from Claim 1 have not been addressed.

A.5. Claim 15

Appellant shows error in the rejection of Claim 15 for the reasons given above with respect to Claim 14 upon which Claim 15 depends.

2 A plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all the claims in the group. See MPEP §707.07(d).

B. GROUND OF REJECTION 2 (Claims 3-4)

B.1. Claim 3

Appellant shows error in the rejection of Claim 3 for the reasons given above with respect to Claim 1 upon which Claim 3 depends.

B.2. Claim 4

Appellant shows error in the rejection of Claim 4 for the reasons given above with respect to Claim 1 upon which Claim 4 depends.

C. GROUND OF REJECTION 3 (Claims 6-7 and 16-19)

C.1. Claim 6

Appellant initially shows error in the rejection of Claim 6 for the reasons given above with respect to Claim 1. Claim 6 includes similar recitations as those contained in Claim 1. For example, Claim 6 also recites a first clock generator and a second clock generator necessary for RFID operation, which none of Kuttruff, Ohkawa, Twitchell Jr. either alone or in combination, discloses or fairly suggests as demonstrated above with respect to Claim 14.

Further, in rejecting Claim 6, the Examiner cites paragraph 0065 for the proposition that Twitchell teaches the processor commands the power block to provide electric power to the RFID module. Appellant urges to the contrary. In the present invention, a battery cell provides electric power to the mobile terminal. A power block provides appropriate electric power to each element of the mobile terminal using the electric power supplied from the battery cell. The power block provides electric power to the RFID chip to enable an operation of each element. The Main Processing Unit (MPU) core informs the power block of an operation time of the RFID chip through an enable pin En. In contrast to the teachings of the present invention as articulated above, Twitchell disclosed:

> In operation, the low power radio frequency (LPRF) communications component 5010 communicates with the reader component 5012 in reading WTs located within the vicinity of the WRT 5008, and the LPRF communications component 5010 receives and transmit data to other WRTs 5008 or to a Gateway 5000 (specifically, the WRT component 5006 of the Gateway 5000). Furthermore, the LPRF communications component 5010 preferably is programmed to power down to an "off" state in order to conserve battery power when the LPRF communications component 5010 no longer is actively transmitting or receiving data packets. The LPRF communications component 5010 also may be capable of powering power down to a standby mode, in which

> case the LPRF communications component 5010 preferably includes a timer circuit or other microprocessor that automatically controls powering up after a predetermined period of time has elapsed since powering down to the standby mode. (emphasis added)(paragraph 0065).

As can be seen, this passage makes no mention whatsoever of any of the specific features recited in Claim 6 such as "a processor connected to the power block, the first clock generator, and the RFID module, for enabling an operation of the power block; and wherein the processor commands the power block to provide electric power to the RFID module, and the RFID module generates the RFID modulation data using the RFID memory, the codec, and the modulator" nor do the teachings of the cited passage cure Kuttruff's deficiency.

It is urged that none of the cited references teach or suggest the claimed feature of "a processor connected to a power block" among others. Thus, it is further shown that Claim 6 has been erroneously rejected under 35 U.S.C. § 103, as there are additional claimed features not taught or suggested by any of the cited references. The Examiner failed to established a prima facie showing of obviousness.

Still further, Appellant has shown error in that the cited reference of Twitchell Jr. is not prior art. Twitchell Jr. was filed as a PCT application and has a 35 U.S.C. § 371 date and 35 U.S.C. § 102(e) date of November 12, 2004, which is after the February 12, 2004 filing date of this pending application.

C.2. Claim 7

Appellant initially shows error in the rejection of Claim 7 for the reasons given above with respect to Claim 6. Claim 6 includes similar recitations as those contained in Claim 7. Although Claim 7 includes similar recitations as those contained in Claim 6 nevertheless the two claims are different. For example, Claim 7 recites "a memory portion for storing the RFID data together with mobile terminal protocol data." However, in the Office Action the Examiner lumped[3] Claims 6 and 7 together and only addressed the limitations of Claim 6; therefore the limitations of Claim 7 that are different from Claim 6 have not been addressed.

3 A plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all the claims in the group. See MPEP §707.07(d).

Appellant has thus shown that there are missing claimed features not taught or, suggested by the cited references, and thus Claim 7 has been erroneously rejected under 35 U.S.C. §103(a). The Examiner has not established a prima facie showing of obviousness.

Still further, Appellant shown error in that the cited reference of Twitchell Jr. is not prior art. Twitchell Jr. was filed as a PCT application and has a 35 U.S.C. § 371 date and 35 U.S.C. § 102(e) date of November 12, 2004, which is after the February 12, 2004 filing date of this pending application.

C.3. Claim 16

Appellant initially shows error in the rejection of Claim 16 for the reasons given above with respect to Claim 6. Claim 6 includes similar recitations as those contained in Claim 16. Although Claim 6 includes similar recitations as those contained in Claim 16 nevertheless the two claims are different. For example, Claim 6 recites "an RFID module including an RFID memory for storing the RFID data; a codec for encoding the RFID data into RFID codec data; a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing a second operation timing to the codec and the modulator" whereas Claim 16 does not. However, in the Office Action the Examiner lumped[4] Claims 6 and 16 together and only addressed the limitations of Claim 6; therefore the limitations of Claim 16 that are different from Claim 6 have not been addressed.

Appellant has thus shown that there are missing claimed features not taught or suggested by the cited references, and thus Claim 16 has been erroneously rejected under 35 U.S.C. §103(a). The Examiner has not established a prima facie showing of obviousness.

Still further, Appellant has shown error in that the cited reference of Twitchell Jr. is not prior art. Twitchell Jr. was filed as a PCT application and has a 35 U.S.C. § 371 date and 35 U.S.C. § 102(e) date of November 12, 2004, which is after the February 12, 2004 filing date of this pending application.

C.4. Claim 17

4 A plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all the claims in the group. See MPEP §707.07(d).

Appellant shows error in the rejection of Claim 17 for the reasons given above with respect to Claim 16 upon which Claim 17 depends.

C.5. Claim 18

Appellant initially shows error in the rejection of Claim 18 for the reasons given above with respect to Claim 6. Claim 6 includes similar recitations as those contained in Claim 18. Although Claim 6 includes similar recitations as those contained in Claim 18 nevertheless the two claims are different. For example, Claim 18 recites "a processor connected to the power block, the first clock generator, the memory portion, and the RFID module, for enabling an operation of the power block, extracting the RFID data, and delivering the extracted RFID data to the RFID module" whereas Claim 6 does not. However, in the Office Action the Examiner lumped[5] Claims 6 and 18 together and only addressed the limitations of Claim 6; therefore the limitations of Claim 18 that are different from Claim 6 have not been addressed.

Appellant has thus shown that there are missing claimed features not taught or suggested by the cited references, and thus Claim 18 has been erroneously rejected under 35 U.S.C. §103(a). The Examiner has not established a prima facie showing of obviousness.

Still further, Appellant has shown error in that the cited reference of Twitchell Jr. is not prior art. Twitchell Jr. was filed as a PCT application and has a 35 U.S.C. § 371 date and 35 U.S.C. § 102(e) date of November 12, 2004, which is after the February 12, 2004 filing date of this pending application.

C.6. Claim 19

Appellant shows error in the rejection of Claim 19 for the reasons given above with respect to Claim 18 upon which Claim 19 depends.

D. GROUND OF REJECTION 4 (Claim 8)

D.1. Claim 8

5 A plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all the claims in the group. See MPEP §707.07(d).

Appellant shows error in the rejection of Claim 8 for the reasons given above with respect to Claim 7 upon which Claim 8 depends.

E. GROUND OF REJECTION 5 (Claim 9)

E.1. Claim 9

Appellant shows error in the rejection of Claim 9 for the reasons given above with respect to Claim 7 upon which Claim 9 depends.

F. GROUND OF REJECTION 6 (Claim 10)

F.1. Claim 10

Appellant shows error in the rejection of Claim 10 for the reasons given above with respect to Claim 7 upon which Claim 10 depends.

CONCLUSION

Appellants have shown multiple errors in the Examiner's final rejection of the claims in the present case. Therefore, based on at least the foregoing, and as the Examiner has failed to make out a prima facie case for an anticipation rejection, the rejection of Claims 1-10 and 14-19 must be reversed.

It is well settled that in order for a rejection under 35 U.S.C. §103(a) to be appropriate, the claimed invention must be shown to be obvious in view of the prior art as a whole. A claim may be found to be obvious if it is first shown that all of the recitations of a claim are taught in the prior art or are suggested by the prior art. *In re Royka*, 490 F.2d 981, 985, 180 U.S.P.Q. 580, 583 (C.C.P.A. 1974), cited in M.P.E.P. §2143.03.

The Examiner has failed to show that all of the recitations of Claims 1, 6, 7, 14, 16 and 18 are taught, disclosed or fairly suggested by either Kuttruff et al., Ohkawa, Pratt, Twitchell, Jenkins IV or Admitted Prior Art (APA), or the combination thereof. Accordingly, the Examiner has failed to make out a prima facie case for an obviousness rejection.

Claims 1, 6, 7, 14, 16 and 18 are not rendered unpatentable by Chalmers, Loving good et al., or Poklemba, or the combination thereof. Thus, independent Claims 1, 6, 7, 14, 16 and 18 are allowable.

Accordingly, dependent Claims 2-5, 8-10, 15, 17 and 19 are allowable because of their dependence upon independent Claims 1, 6, 7, 14, 16 and 18.

Appellants respectfully request that the Board reverses such final rejection.

By:

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Attorney For Applicant

Dated: June 20, 2007

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CLAIMS APPENDIX

The text of the claims involved in the appeal is:

1. (Original) A mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising:

an antenna for communicating with the RFID reader;

a memory portion for storing the RFID data together with mobile terminal protocol data;

a codec for encoding the RFID data into RFID codec data;

a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data;

a processor connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec;

a detector connected to the antenna and the processor, for informing the processor of an approach of the RFID reader;

a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion; and

a second clock generator connected to the first clock generator, the codec, and the modulator, for providing operation timing to the codec and the modulator.

2. (Original) The mobile terminal circuit of claim 1, wherein the processor extracts the RFID data from the memory portion in response to information indicating the approach of the RFID reader, provided from the detector, and delivers the extracted RFID data to the codec.

3. (Original) The mobile terminal circuit of claim 1, wherein the detector includes an interrupt port of the processor.

4. (Original) The mobile terminal circuit of claim 1, wherein the detector includes a frequency detector.

5. (Original) The mobile terminal circuit of claim 1, further comprising a rectifier for rectifying a voltage detected from a signal received via the antenna and delivering the rectified voltage to the processor.

6. (Original) A mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising:

an antenna for communicating with the RFID reader;

a first clock generator for providing a first operation timing to each electric element of the mobile terminal circuit;

an RFID module including an RFID memory for storing the RFID data; a codec for encoding the RFID data into RFID codec data; a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing a second operation timing to the codec and the modulator;

a power block for providing operation power to electric elements of the mobile terminal circuit;

a processor connected to the power block, the first clock generator, and the RFID

module, for enabling an operation of the power block; and

a detector connected to the antenna and the processor, for informing the processor of an approach of the RFID reader;

wherein the processor commands the power block to provide electric power to the RFID module, and the RFID module generates the RFID modulation data using the RFID memory, the codec, and the modulator.

7. (Original) A mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising:

an antenna for communicating with the RFID reader;

a first clock generator for providing a first operation timing to each electric element of the mobile terminal circuit;

a memory portion for storing the RFID data together with mobile terminal protocol data;

an RFID module including a codec for encoding the RFID data into RFID codec data; a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing a second operation timing to the codec and the modulator;

a power block for providing operation power to the electric elements of the mobile terminal circuit;

a processor connected to the power block, the first clock generator, the memory portion, and the RFID module, for enabling an operation of the power block, extracting the RFID data, and delivering the extracted RFID data to the RFID module; and

a detector connected to the antenna and the processor, for informing the processor of an

approach of the RFID reader;

wherein the processor commands the power block to provide electric power to the RFID module, and the RFID module generates RFID modulation data by encoding and modulating the received RFID data.

8. (Original) The mobile terminal circuit of claim 7, wherein the processor commands the power block using an enable pin.

9. (Original) The mobile terminal circuit of claim 7, wherein the detector is included in the processor.

10. (Original) The mobile terminal circuit of claim 7, wherein the detector includes a frequency detector for detecting a variation in frequency.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Original) A mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising:

an antenna for communicating with the RFID reader;

a memory portion for storing the RFID data together with mobile terminal protocol data;

an RFID module for performing an RFID function and including a second clock generator for providing RFID operation timing using a system clock output from a first clock generator;

a processor connected to the memory portion and the RFID module, for extracting the RFID data stored in the memory portion and delivering the extracted RFID data to the RFID module; and

a detector connected to the antenna and the processor, for informing the processor of an approach of the RFID reader;

wherein the first clock generator is connected to the processor and the memory portion, and provides operation timing to the processor and the memory portion.

15. (Original) The mobile terminal circuit of claim 14, wherein the RFID module includes a codec for encoding the RFID data into RFID codec data; and a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data.

16. (Original) A mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising:

an antenna for communicating with the RFID reader;

a first clock generator for providing a first operation timing to each electric element of the mobile terminal circuit;

an RFID module for performing an RFID function;

a power block for providing operation power to the electric elements of the mobile

terminal circuit;

a processor connected to the power block, the first clock generator, and the RFID module, for enabling an operation of the power block; and

a detector connected to the antenna and the processor, for informing the processor of an approach of the RFID reader;

wherein the processor commands the power block to provide electric power to the RFID module, and the RFID module generates the RFID data.

17. (Original) The mobile terminal circuit of claim 16, wherein the RFID module includes an RFID memory for storing the RFID data; a codec for encoding the RFID data into RFID codec data; a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing a second operation timing to the codec and the modulator.

18. (Original) A mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising:

an antenna for communicating with the RFID reader;

a first clock generator for providing a first operation timing to each electric element of the mobile terminal circuit;

a memory portion for storing the RFID data together with mobile terminal protocol data;

an RFID module for processing the RFID data;

a power block for providing electric power to the electric elements of the mobile terminal

circuit;

a processor connected to the power block, the first clock generator, the memory portion, and the RFID module, for enabling an operation of the power block, extracting the RFID data, and delivering the extracted RFID data to the RFID module; and

a detector connected to the antenna and the processor, for informing the processor of an approach of the RFID reader;

wherein the processor orders the power block to provide the electric power to the RFID module, and the RFID module generates the RFID data.

19. (Original) The mobile terminal circuit of claim 18, wherein the RFID module includes a codec for encoding the RFID data into RFID codec data; a modulator connected to the codec, for modulating the RFID codec data into RFID modulation data; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing a second operation timing to the codec and the modulator.

EVIDENCE APPENDIX

There is no evidence to be presented.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.